REMARKS

In the Office Action mailed March 13, 2007 the Examiner noted that claims 1-4, 9-13, 15-18, 23-37, and 29-32 were pending and rejected claims 1-4, 9-13, 15-18, 23-37, and 29-32. Claims 1, 9-13, 15, 23-27 and 29-32 have been amended, no claims have been canceled, no new claims have been added and, thus, in view of the forgoing claims 1-4, 9-13, 15-18, 23-37, and 29-32 remain pending for reconsideration which is requested. No new matter has been added. The Examiner's rejections are traversed below.

REJECTIONS under 35 U.S.C. § 112

Claims 1-4, 9-13, 15-18, 23-27, 29 and 30 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. Specifically, the Examiner states that the specification fails to disclose mirror area of a first module. Claim 1, 13, 15, 27, 29 and 30 have been amended to use the phrase "said mirror area of said one second module." Support for the amendment found on page 15 lines 10 through page 16 line 4.

Claims 1-4, 9-13, 15-18, 23-27 and 29-32 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In particular the Examiner states that "said mirror area of said one first module" lacks antecedent basis in claims 1, 13, 15, 27, 29 and 30. The claims have been amended to recite "a mirror area of said one second module."

With respect to claim 32, the Examiner states that "running short of space," is a relative term. Claim 32 has been amended to recite "a first memory module is insufficient for a data input request." Support for the amendment found on page 10 lines 21-25. Insufficient for a data input request is submitted to be inherent from the term "runs short". Also see, Merriam-Webster online dictionary for the definition of short, http://www.m-w.com/dictionary/short. The word short bring defined as:

> **5 a :** not coming up to a measure or requirement **:** INSUFFICIENT <in *short* supply> **b :** not reaching far enough <the throw to first was *short*> **c :** enduring privation **d :** insufficiently supplied <*short* of cash> <*short* on brains>

As to claim 31, the Examiner states that the phrase "a write of data to a master area of a first management module written to a mirror area of a second management module," renders the claim indefinite. Claim 31 has been amended to render the claim language definite.

REJECTIONS under 35 U.S.C. § 102

Claim 32 is rejected under 35 U.S.C. § 102(e) as anticipated by Avraham, U.S. Patent Pub. No. 20040103238. Avraham discusses a flash memory unit that provides a volatile memory that has the contents of the volatile memory written to a non-volatile memory when a power interruption occurs. Avraham paragraph 0054 states:

> FIG. 3 is a flowchart that illustrates the operation of the present invention constructed according to any of FIGS. 1 through 2B. Operation starts in block 300 when host device 120/120A/120B/120C is turned on. Step 301 covers the nominal operation of the system, which includes in block 302 **writing user data to non-volatile memory module** 112 and/or reading user data from non-volatile memory module 112, while in **block 303 system data is cached in and/or read from volatile memory module** 113. Caching in block 303 may lead volatile memory module 113 to become full, which condition is examined in step 305. **If volatile memory module 113 is indeed full, then in step 309 all or part of the content of volatile memory 113 are copied to nonvolatile memory** 112, and the freed memory volatile space is cleared for further caching. An example of a case in which the cache is partially emptied is when user data buffered in the cache is copied to the nonvolatile memory and cleared, while system data remains in the cache.

Thus, Avraham discusses copying data from the volatile memory to the non-volatile memory when the volatile memory is full. It does not teach or suggest redirecting the storing from the master of the first module to the mirror of the second when the master area of the first memory module is full. Therefore, Avraham does not teach or suggest "storing data initially directed to the master area of a first memory module in a mirror area of a second memory module," as in amended claim 32.

REJECTIONS under 35 U.S.C. § 103

Claims 13, 27 and 30 stand rejected under 35 U.S.C. § 103(a) as being obvious over Weber, U.S. Patent No. 5,937,174 in view of Hauck, U.S. Patent Pub. No. 20030158999, in further view of Avraham. Weber is directed to a cache memory control architecture within a RAID storage system. Hauck is a method of retaining cache coherency in a controller. In contrast the present claims are directed to a dual cache memories accessed by a single address destination.

As stated above, Avraham does not teach or suggest redirecting the storing from the master of the first module to the mirror of the second when the master area of the first memory module is full. Therefore, it does not teach "a master area of said one second module and a mirror area of said other second module are written to until the master area of said one second

module is full, at which time a mirror area of said one second module are written," as in amended claims 13, 27 and 30.

Further, at page 9 of the Examiner states that Hauck nor Weber teach the feature discussed above, but that Avraham does. In particular, the Examiner at page 10 of the Office Action states:

> It would have been obvious to one of ordinary skill in the art at the time of the invention for Weber to further include Avraham's appliance including a FLASH memory in to his own scalable memory. By doing so, Weber would have a more robust memory system, capable of increasing the efficiency and reducing wear in case of a catastrophic system failure as taught by Avraham in paragraphs 0005 through 0006, all lines.

The purpose of the redundant memory controller (Fig. 6 Hauck) is to allow a system to keep on running when a failure occurs. If a FLASH memory was added to Hauck as the Examiner asserts, the failed controller which had stored its contents in the FLASH memory, would have to purge that stored info on re-initialization as the memory controller that continued to function would have more up to date data. Therefore, the FLASH memory servers no purpose and thus, the references teach away from combination. Further, as the combination serves no purpose, the added cost of FLASH memory would make the resulting combination more expensive.

Further, claims 13, 27, and 30 recite in part:

> wherein, in a case in which a capacity of a master area of said cache memory of the one second module is full when data to be read out through said bridge module into said first module is temporarily preserved in the cache memory of the one second module, the one second module preserves the readout data in a mirror area of said cache memory of the other second module on the basis of a situation of management by said manager.

Examiner cites Hauck, Paragraph 0054-0056 as teaching the limitation. The current claims teach a method of efficiently using the cache. While Hauck discusses, a method of performing failover from one controller 720, to a replacement controller 730. With paragraph 0054 discussing which of the controllers can own particular cache lines. In contrast, the present claims discuss writing to a master area of a cache and the mirror area of a different cache and only when the master area of the first cache is full starting writing in the master area of a second cache. Therefore, Hauck does not teach a "capacity of a master area of said cache memory of the one second module is full when data to be read out through said bridge module into said first module is temporarily preserved in the cache memory of the one second module …"

For the reasons stated above, Weber, Hauck and Avraham taken separately or in

combination fail to teach or suggest the elements of claims 13, 27, and 30.

Claim 1-4, 9-12, 15-18, 23-26 and 29 stand rejected under 35 U.S.C. § 103(a) as being obvious over Weber in view of Hauck and Avraham in further view of Hashimoto, U.S. Patent Pub. No. 20020016898. Hashimoto discusses an interface circuit performing data transmission between an external host controller and an external device.

Hashimoto paragraph 0064 discusses generation of two specific addresses used for continuous access to a series of areas, it is not writing to two mirrored cache areas. Therefore, Hashimoto does not disclose "address production means for analyzing said addressing information, which is received together with said data to be written from said first module, to produce two transferred-to addresses for designation of said two second modules having said cache memories in which said data is to be actually written and to produce written-in addresses in said cache memories," of claim 1.

For the reasons stated above, Weber, Hauck, Avraham and Hashimoto do not teach or suggest the elements of claims 1, 15 and 29 and the claims dependent therefrom.

As regards dependent claims 9-12 and 23-26, nothing cited or found in Hauck suggests a master area of a cache memory. While the present claims have a mirror area, the mirror area is not analogous to the master area, and therefore, Hauck does not teach "wherein, in a case in which a capacity of a master area of said cache memory of the one second module is full when data to be read out through said bridge module into said first module is temporarily preserved in the cache memory of the one second module, the one second module preserves the readout data in a mirror area of said cache memory of the other second module on the basis of a situation of management by said management means," as recited in claim 9.

As regards, dependent claims 4 and 18, the Examiner states on pages 15 and 16 of the Office Action:

> It is worthy to note that since Weber only teaches one bus line, the address generated by Hashimoto could only refer to the one address bus that is used to transfer the data specified by the generated address.

Thus, Examiner admits that the combination of Weber and Hashimoto do not teach or suggest numbers specifying the PCI bus for each bus. Therefore, Weber, Hauck, Avraham and Hashimoto fail to teach or suggest "wherein said interface bus is a PCI (Peripheral Component Interconnect) bus, and numbers for specifying said PCI bus for said two second modules are designated as said specific information," as in claims 4 and 18.

Weber, Hauck, Avraham and Hashimoto do not teach or suggest the elements of claims 9-12 and 23-26. Withdrawal of the rejection is respectfully requested.

It is submitted that the claims satisfy the requirements of 35 U.S.C § 112 It is also submitted that claims 1-4, 9-13, 15-18, 23-37, and 29-32 continue to be allowable. It is further submitted that the claims are not taught, disclosed or suggested by the prior art. The claims are therefore in a condition suitable for allowance. An early Notice of Allowance is requested.

If any further fees, other than and except for the issue fee, are necessary with respect to this paper, the U.S.P.T.O. is requested to obtain the same from deposit account number 19-3935.

Respectfully submitted,

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